Laser guide star optimized wavefront sensor system for the Thirty Meter Telescope

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ABSTRACT

As part of the adaptive optics (AO) system NFIRAOS for the Thirty Meter Telescope (TMT), TMT is developing Shack Hartmann wavefront sensor cameras optimized for laser guide star (LGS) AO. NFIRAOS will use six of these cameras in its multi-conjugate AO system for LGS AO, and one for a natural guide star pyramid wavefront sensor. Called VCAM (Visible wavelength CAMera), the wavefront sensor camera system is being developed for TMT by Astronomical Research Cameras, Inc. The LGS AO cameras use a novel CCD design called the polar coordinate detector (designated the CCID87) being developed for TMT by the Lincoln Laboratory of the Massachusetts Institute of Technology. The polar coordinate detector matches individual imagers in each subaperture to the size and orientation of the perspective elongation of the sodium laser guide star image across the 30 m telescope aperture. The detector has 128 video outputs, each of which must be read out at a 2 KHz frame rate. VCAM integrates all the electronics in a compact package and provides a 10 Gbit/s optical data link for transmission of wavefront measurements to the NFIRAOS real time computer. In this paper we describe the design of the CCID87 and VCAM and discuss the testing of the CCID87 and the VCAM prototype.

Keywords: Adaptive optics, Shack Hartmann, wavefront sensing, laser guide star

1. LGS AO WAVEFRONT SENSING FOR NFIRAOS

The Thirty Meter Telescope (TMT) adaptive optics (AO) system NFIRAOS[1] uses six laser guide stars and six Shack Hartmann wavefront sensors with 60 x 60 subapertures to sense the atmospheric turbulence above the telescope. The lasers operate at wavelengths optimized for excitation of the rarified strata of sodium atoms present in the earth's mesosphere at approximately 90 km altitude. The lasers excite the sodium atoms causing them to emit light by spontaneous emission.

The TMT laser guide star (LGS) facility projects the laser beams used to form the laser guide stars from a projection system located behind the TMT's secondary mirror. The Shack Hartmann wavefront sensor's subapertures correspond to 50 cm square samples of the 30 meter diameter TMT pupil, with the center of the outermost subapertures located 14.75 m from the center of the telescope aperture. Subapertures nearest the center of the telescope aperture see a LGS image that corresponds to the shape (nominally circular) of the projected laser beam. In contrast, subapertures at the outer edges of the pupil see an illuminated column in the mesospheric sodium layer, this is illustrated in Figure 1. The angular extent of the LGS image θ is a function of the thickness of the sodium layer ΔL, the distance to the sodium layer L, and the distance d of the subaperture from the laser projection point, which in this case is the center of the telescope aperture.

Figure 2 shows a portion of the telescope aperture overlaid with the 60 x 60 subaperture pattern. Note that the subapertures blocked by the telescope's central obscuration are omitted, as are the subapertures that fall outside of the essentially circular telescope aperture. The dashed line in the figure crosses through the center of two subapertures, one near the center of the telescope aperture and one at the outer edge. The relatively unelongated image near the center is illustrated by an orange circle, and the elongated image at the outer edge is illustrated by an ellipse. Note that the long axis of the elongated image points towards the center of the telescope aperture, which is also the laser projection point as already noted.

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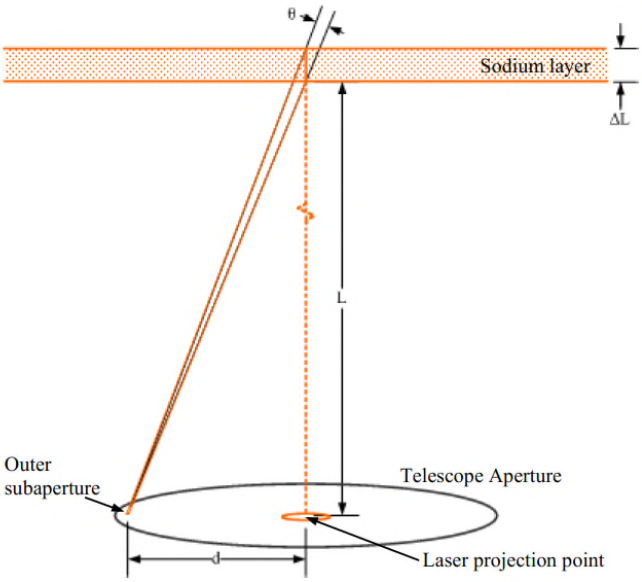

Figure 1: Perspective elongation of the LGS image

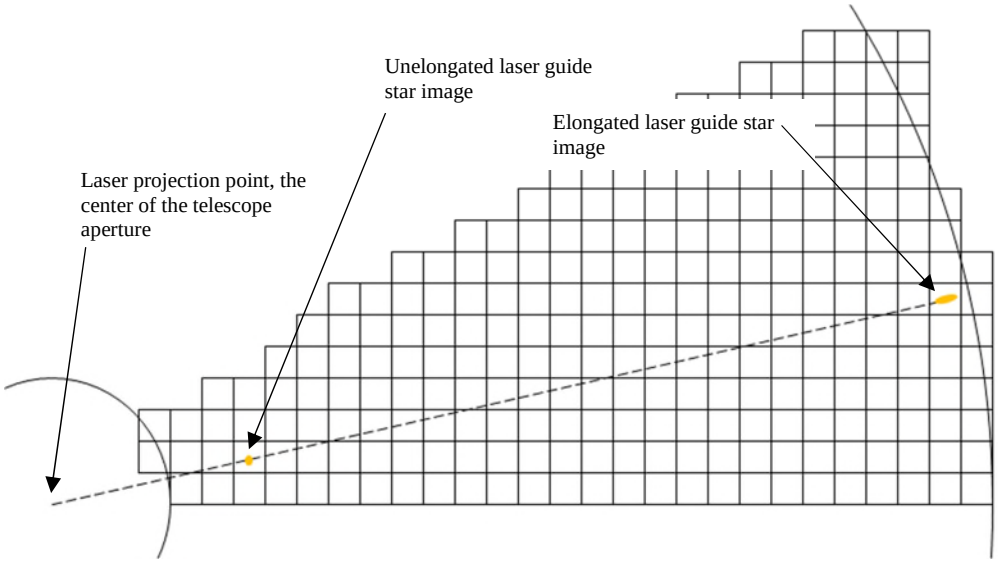

Figure 2: Example LGS images on a portion of the Shack Hartmann subaperture array

Proper operation of the Shack Hartmann wavefront sensor requires that the image in each subaperture is not truncated because of image elongation or image displacement. It must be kept in mind that the sodium layer thickness varies (from ~10 km to ~20 km) both during the night and seasonally, so the wavefront sensor's detector must provide enough pixels to accommodate a varying image size in the elongation direction in order to avoid truncation of the LGS image.

The optimal pixel scale for the Shack Hartmann wavefront sensor depends on the size of the LGS image. The total size of the pixel array in a subaperture needs to consider the amount of elongation as well as an allowance for operation off the null point for calibration of the wavefront sensor and compensation for non-common path errors between the AO system and the science instruments. With a pixel scale of 0.5 arcseconds, the innermost subapertures, where the LGS image is not significantly elongated require 6 x 6 pixels. For the outer most subapertures, the elongation direction requires 15 pixels.

If we plan to employ a conventional CCD, then we need to allocate a minimum of 15 x 15 pixels to each subaperture. For the 60 x 60 subaperture Shack Hartmann wavefront sensor we then need a minimum CCD size of 900 x 900 pixels. A detector of this size might seem reasonable until other performance considerations are included. For the Shack Hartmann

wavefront sensor two of the principal considerations are the frame rate of the wavefront sensor, and the wavefront measurement error due to detector read noise. NFIRAOS will operate at an 800 Hz frame rate in LGS mode, and for a 900 x 900 pixel detector this will lead to high pixel rates for detector readout and in turn higher read noise.

The polar coordinate detector[2][3] was conceived as a solution to the problem presented by perspective elongation in a Shack Hartmann wavefront sensor for LGS AO on an extremely large telescope. The design of the detector recognizes that the elongated image in each subaperture falls on only a small number of pixels with the long dimension of the elongated image pointing toward the center of projection, in this case the center of the Shack Hartmann wavefront sensor detector. In addition, the amount of elongation is essentially none in the innermost subapertures, and increases as the subapertures are located farther from the center of the detector. The frame rate vs. read noise tradeoff is addressed by designing the detector so that each subaperture has only the number of pixels needed for the size of the image, with the innermost subapertures having 6 x 6 pixels. The size of one axis of the subaperture imagers increases to the maximum of 15 pixels as the distance to the center of the detector increases. The pixel arrays in each subaperture are all oriented so that their long axis is aligned with the direction of elongation of the LGS image in each subaperture.

In the design of the detector providing imagers optimized for each of the Shack Hartmann wavefront sensor subapertures we can also choose to omit the subapertures in the 60 x 60 configuration that are not illuminated. When the central obscuration and the nominally circular telescope aperture are considered this reduces the number of imagers required from 3,600 to 2,896. With the variable size subaperture imagers the total number of pixels required is then 204,792 instead of the 810,000 pixels required for a conventional CCD layout.

There are three other important benefits that come from the polar coordinate detector design. One is that with the long dimension of the pixel array matched to the direction of elongation, the extra pixels provide sampling of the variations in the density of the sodium layer, a feature revealed by perspective elongation that can be used to advantage in more advanced image centroiding algorithms. A second benefit is that if the row to row transfer direction of the imager is organized so that the apparent motion of a short duration laser pulse which moves along the elongation axis is tracked by row to row transfers, then the elongation of the LGS image is eliminated[2]. Finally, since the imager array is very small compared to the subaperture pitch, there is room to include a light shielded frame store in each subaperture. This frame store allows a longer integration time in each frame by allowing read out to take place in parallel with imaging of the next frame. The frame store also provides a place to “hide” the image between laser pulses to avoid seeing the Rayleigh scattering of the laser light at the lower altitudes above the telescope.

2. THE CCID87 POLAR COORDINATE DETECTOR

The CCID87 implements the polar coordinate detector design for a 60 x 60 subaperture Shack Hartmann wavefront sensor optimized for the LGS wavefront sensing requirements of NFIRAOS. The CCID87 is being developed for TMT by the Lincoln Laboratory of the Massachusetts Institute of Technology (MIT/LL). The design of the detector is based on a prototype device designated the CCID61[3] which implemented one quadrant of the rotationally symmetric layout required for the center laser projection configuration chosen for the TMT. The configuration of the subapertures by size (from 36 to 90 pixels per subaperture) is shown in Figure 3. There are ten different sizes of subaperture, each located on a 0.5 mm pitch, corresponding to the 50 cm sampling of the telescope pupil with a 1000:1 focal reduction.

The design of a 6 x 15 pixel imager is shown in Figure 4. The imaging array is located at the center of the subaperture, with the row axis of the imager (15 pixels long) oriented so that it points at the center of the detector. The orange ellipse on the imaging array illustrates the elongated LGS image. Adjacent to the imaging array is an identically sized frame store. The end of the imager opposite the frame store provides a charge dump drain for quick clearing of charge from the imager. The row axis of the imager and frame store is rotated around the center of the subaperture as the location of the subaperture changes around the 360 degree circle covered by the polar coordinate detector’s subaperture imagers.

The isolation of the imagers in each subaperture presents a problem for transferring the image charge to the CCD video outputs. After consideration of a row and column multiplexing arrangement, which had the potential for performance problems, both in noise and speed, the concept was developed of a long serial register that “snaked” from one subaperture to another. A sample of the CAD layout for the device is shown in Figure 5. This shows several subaperture imagers and frame stores with the serial register connecting to each frame store and then snaking on to the next subaperture’s frame store.

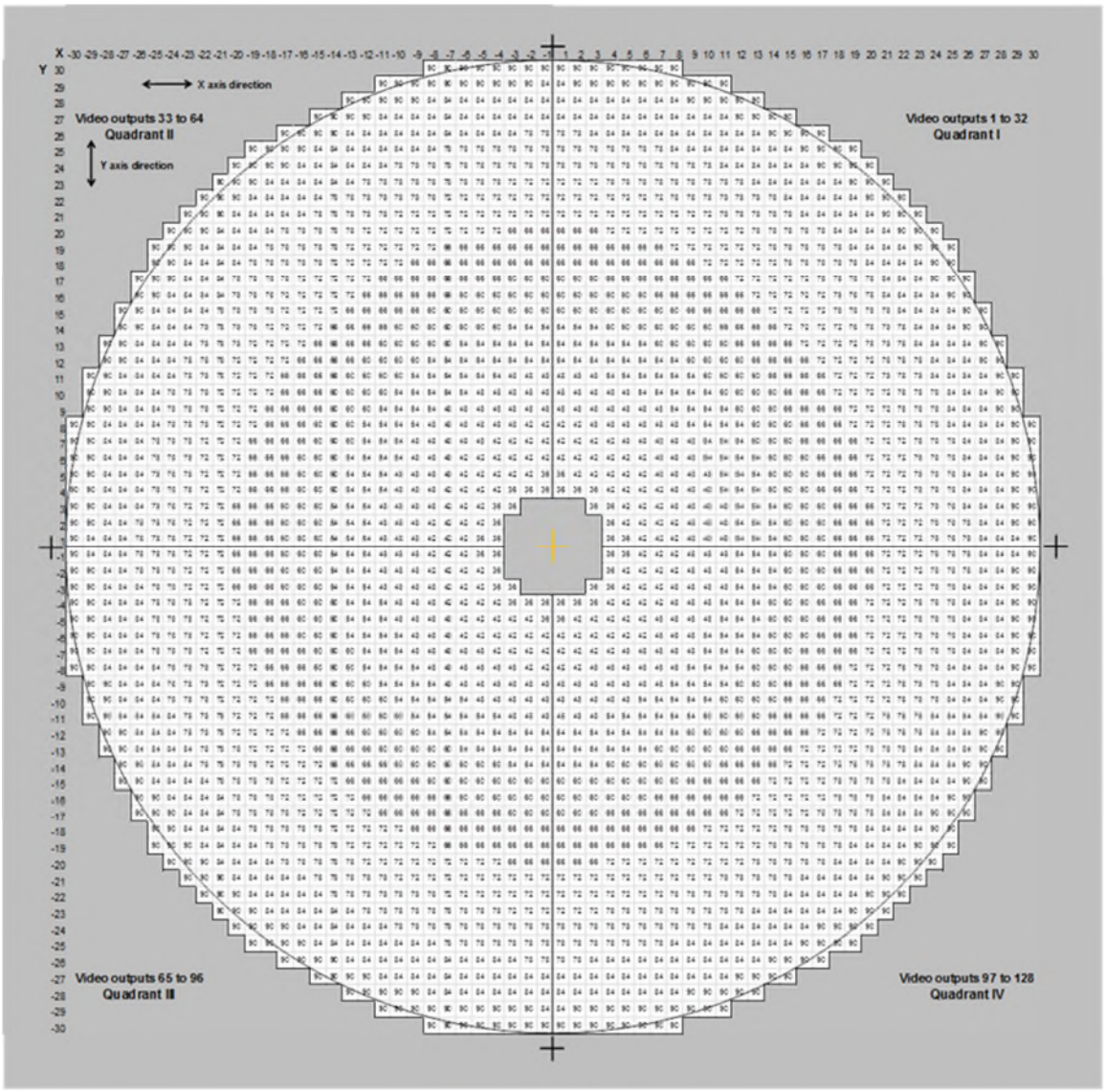

Figure 3: CCID87 subaperture configuration

The imager and frame store use three phase clocks, while the serial register uses a two phase clock. The two phase clock simplifies the serial register clock routing and has been demonstrated to allow higher speed operation with excellent charge transfer efficiency. Although the NFIRAOS LGS AO frame rate is only 800 Hz, the real time computations will run fast enough to allow processing an image frame and the delivery of new deformable mirror commands within one frame time if the detector can be read out in 500 µs or less, equivalent to a 2,000 Hz frame rate.

The serial register is also provided with a charge dump drain to allow rapid clearing. Each serial register makes its way from the center of the detector to the outer edge where it terminates at the video output structure. The video output structure incorporates a novel sense node design consisting of a planar P type JFET that provides high responsivity.

A trade study was performed to optimize the number of video outputs and the length of the serial registers, with the goal of keeping the number of pixels roughly equal in every serial register since the readout time will be determined by the longest serial register. This resulted in a design with 128 video outputs, 32 for each quadrant of the detector.

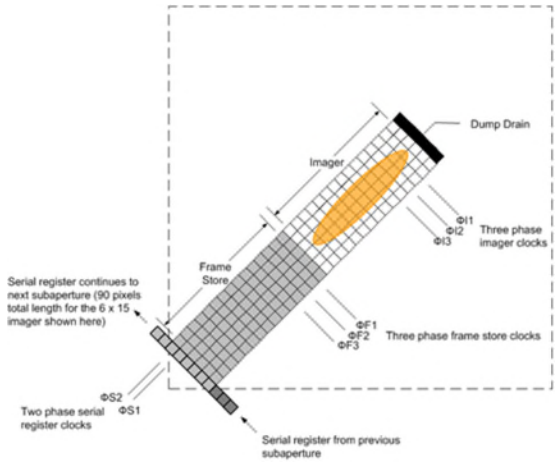

Figure 4: 6 x 15 pixel imager and frame store layout

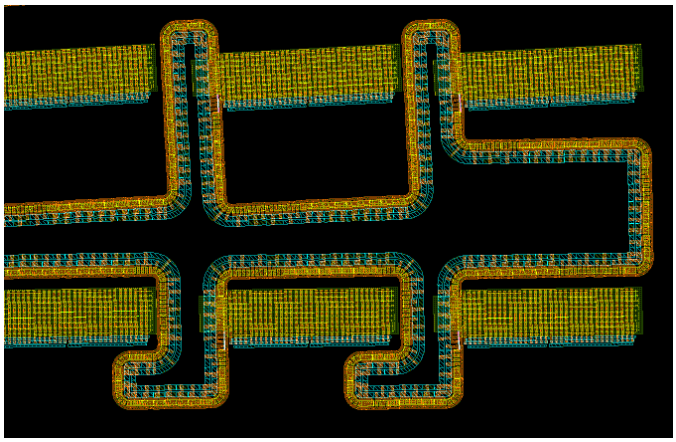

Figure 5: Subaperture and serial register layout detail

The serial register layout must provide the correct number of pixels to hold the charge from each imager, which varies along its length as the serial register goes from the center of the detector (36 pixel imagers) to the outside (90 pixel imagers). This requires more transfers from the frame store into the serial register for the larger imagers, creating the necessity to provide separate frame store clocks for each of the 10 different sized subapertures, as illustrated for one quadrant of the detector in Figure 6. To support pulse tracking, there are also 10 different sets of imager clocks since for a pulsed laser, the speed at which the LGS image spot moves is a function of the distance of the subaperture from the center of the detector.

When the imager, frame store and serial register clocks, along with clocks specific to the video outputs and the charge dump facilities are counted, the device has a total of 66 clock inputs.

The CCID87 Layout

The completed CAD layout of the CCID87 is shown in Figure 7. The rotational symmetric arrangement is clearly visible. The video outputs are in the four corners of the layout, isolating them from the clock signals which enter the layout along each edge. The design requires three layers of metal to allow for all the interconnections with no gaps or seams between the quadrants. The three metal layers are indicated in the CAD layout by the aqua, blue, and purple colors.

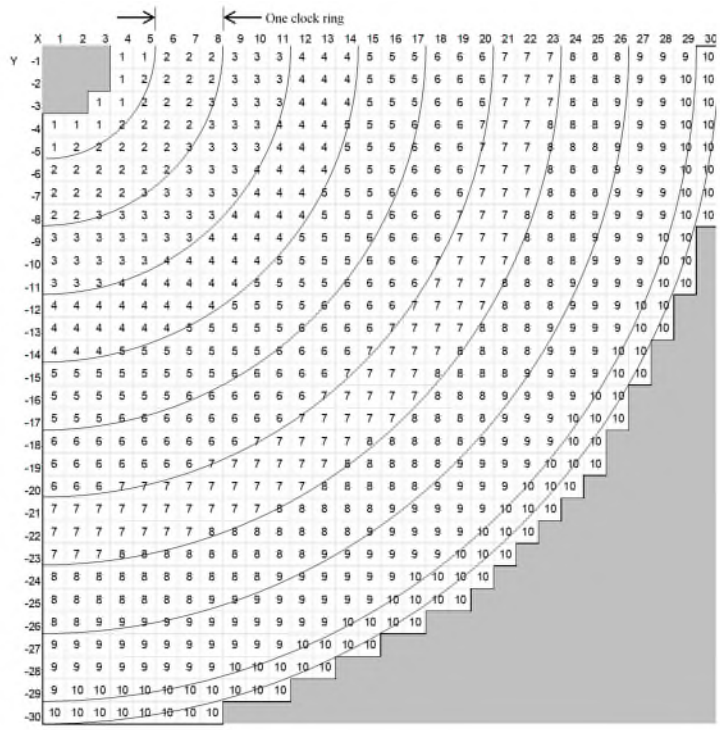

Figure 6: Imager and frame store clock assignments for one quadrant of the CCID87

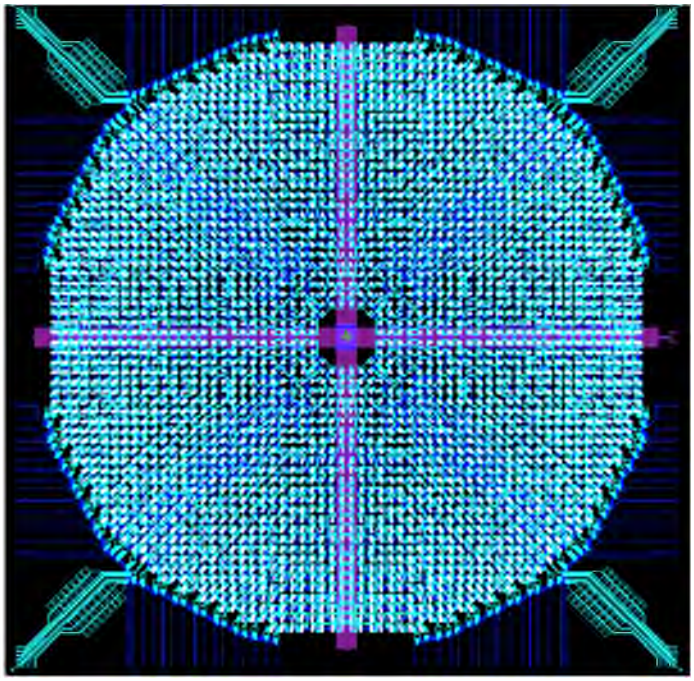

Figure 7: CCID87 layout

Images of finished CCID87 wafers are shown in Figure 8. The left side shows a wafer after completion of front illumination processing, and the right side of the figure shows a wafer after completion of back illumination processing. There are 14 complete devices per wafer. As noted earlier the subaperture imagers are small compared to the pitch of the subapertures. Normally the area of the device outside of the imagers is covered with an aluminum light shield as part of back illumination processing to protect the frame store and serial registers from light. For the CCID87 this would result in serious problems with unwanted reflections between the CCD and any optical surfaces before it (particularly the package window and the

lenslet array). This led to the development of a special black dielectric coating for the CCID87 as shown on the right side of Figure 8.

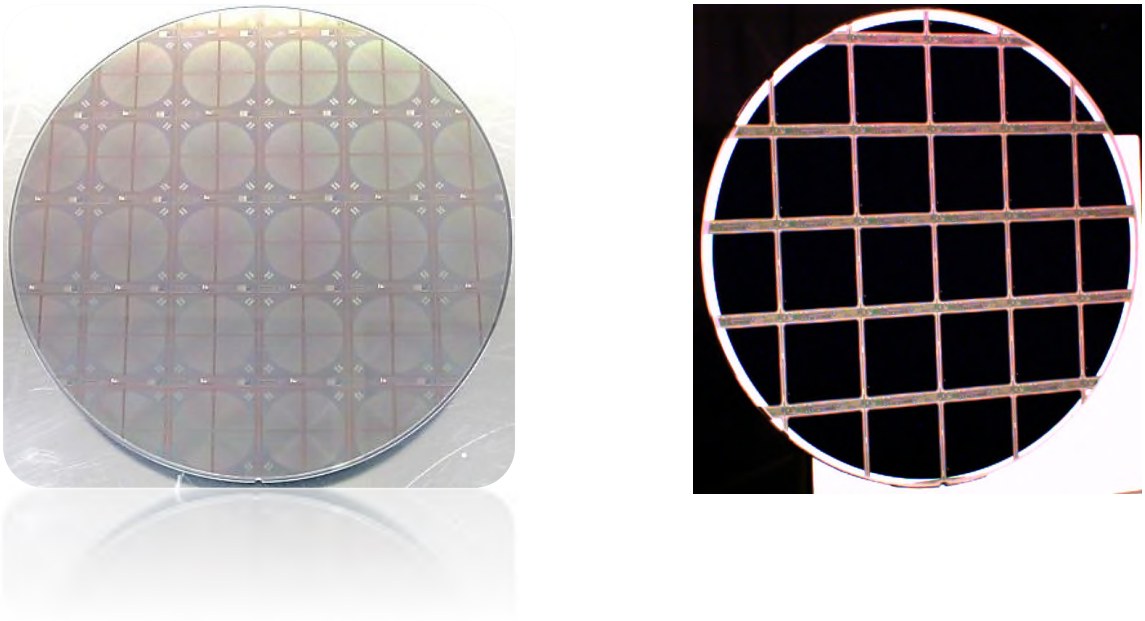

Figure 8: Finished front (left side) and back (right side) illuminated CCID87 wafers. Note that the white areas in the right image are from far off-axis illumination.

The CCID87 is packaged in a hermetic, windowed 480 pin PGA package with an integral thermoelectric cooler (TEC). The body of the package is shown in Figure 9. The package is alumina ceramic with a mounting ring made of Kovar. The left side of the figure shows the inside of the package, and the right side of the figure shows a bottom view of the package. The TEC is mounted inside the package on top of a Copper-Tungsten heat sink foot. A ceramic interposer circuit board is mounted on top of the TEC and the CCID87 is epoxied to the interposer. Bond wires connect the CCID87 to the interposer, and the interposer is connected by bond wires to an array of pads surrounding the inside cavity of the package that connects to the package pins. A sapphire package window mounts in a bezel that is laser welded into a recess in the package seal ring.

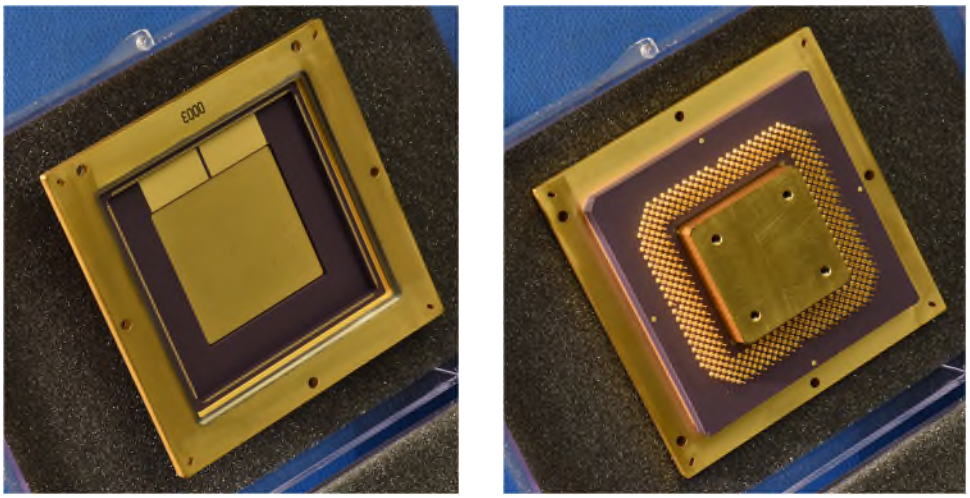

Figure 9: 480 pin PGA package

CCID87 Specifications

The specifications of the CCID87 are summarized in Table 1.

• 60 x 60 subapertures on a 500 µm x 500 µm grid	• 25,000 e- full well
• 2,896 subapertures, 6 x 6 to 6 x 15 pixels	• QE > 95% at 589 nm
• 204,792 10.5 µm x 10.5 µm pixels	• Windowed hermetic package
• 128 video outputs	• Integral TEC for device operation down to -30 °C
• 3.6 MHz pixel readout rate with < 3.5 e- read noise, supporting an AO frame rate of 800 Hz with no latency	• Non-reflective coating outside of the active imaging areas

Table 1: CCID87 summary specifications

CCID87 Status

Testing of the first 8 wafers at front illumination has been completed, and testing of back illuminated wafers is in progress. Fully functional science grade devices have been obtained, although yield has been lower than expected. An example of an illuminated and dark frame frontside test image is shown in Figure 10. The images were taken at room temperature, and the image shows each subaperture image without rotating the images to match the actual orientation of the imager in each subaperture. The non-uniformity of the illuminated frontside test image is due to obscuration of the subapertures by the metal layers at the top of the frontside layers.

There are 8 additional wafers undergoing front illumination testing, and a second lot of 16 wafers is also being fabricated.

The next steps for the CCID87 are to complete back illumination processing of the remaining 8 wafers from the first lot, complete the second lot, and package engineering and science grade devices. A total of 16 science grade devices will be delivered.

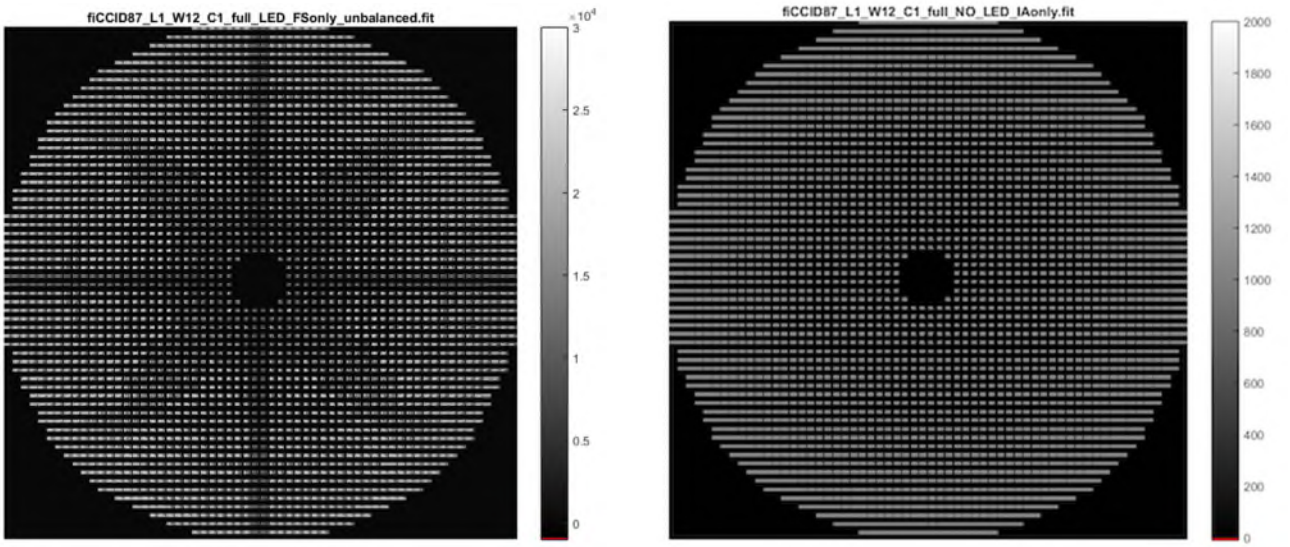

Figure 10: CCID87 frontside test images. The left hand image is illuminated and the right hand image is a dark frame at +20 °C (metallization obscures portions of subapertures and in this display the subaperture images are not rotated to match the actual polar coordinate orientation).

3. VCAM

The NFIRAOS wavefront sensor camera is called VCAM (Visible wavelength CAMera). There are two versions of VCAM, one is the LGS wavefront sensor and this version uses the CCID87 polar coordinate detector and a 60 x 60 lenslet array. The other version of VCAM is the natural guide star (NGS) wavefront sensor for NFIRAOS. The NGS version uses a conventional 256 x 256 pixel CCD[4] also developed in collaboration with MIT/LL and designated the CCID74.

The design of VCAM addresses the challenges presented by the CCID87 and by operating within NFIRAOS. Interconnection of the 128 video outputs of the CCID87 with remotely located camera electronics would present serious problems for signal integrity and the complexity of the connections. The goal of low read noise would also be compromised by remote location of the electronics. This leads to a design where the electronics and the detector are integrated into a camera assembly. This is made more difficult by the fact that the cameras will be located inside the NFIRAOS optical enclosure which is cooled to -30 °C to reduce the thermal background of the AO system in the near IR. The camera is not allowed to dissipate any significant heat into the enclosure because the resulting convection currents would disturb the AO system's optical path.

TMT selected Astronomical Research Cameras (ARC) of San Diego, CA[5] to develop VCAM after a competitive request for quotation process. The electronic design of VCAM is an evolution of the most recent ARC product, the Generation IV (GEN IV) system which supports up to 64 channels for the readout of infrared focal plane arrays. The major changes to produce the VCAM electronics are the development of video processing electronics for CCD readout, scaling of the GEN IV video boards from 16 channels per board to 32, integral control of the TEC in the detector package, and adoption of a standard Ethernet link for camera control and a separate 10 Gbit/s Ethernet link for transmission of image data to the NFIRAOS real time computer system (RTC).

The opto-mechanical design of VCAM is illustrated in Figure 11. The electronics consist of circuit boards stacked inside of an aluminum cold plate assembly that is in turn contained within a main housing made of aluminum. A rear cover provides mounting for a DC power input connector, fiber optic connections for the control and image data links, a frame trigger signal input, and connections for a coolant supply and return. The coolant circulates through the cold plate assembly that surrounds the circuit cards on all four sides. The coolant also circulates through a heat sink attached to the back of the CCD package and takes away the heat generated by the TEC.

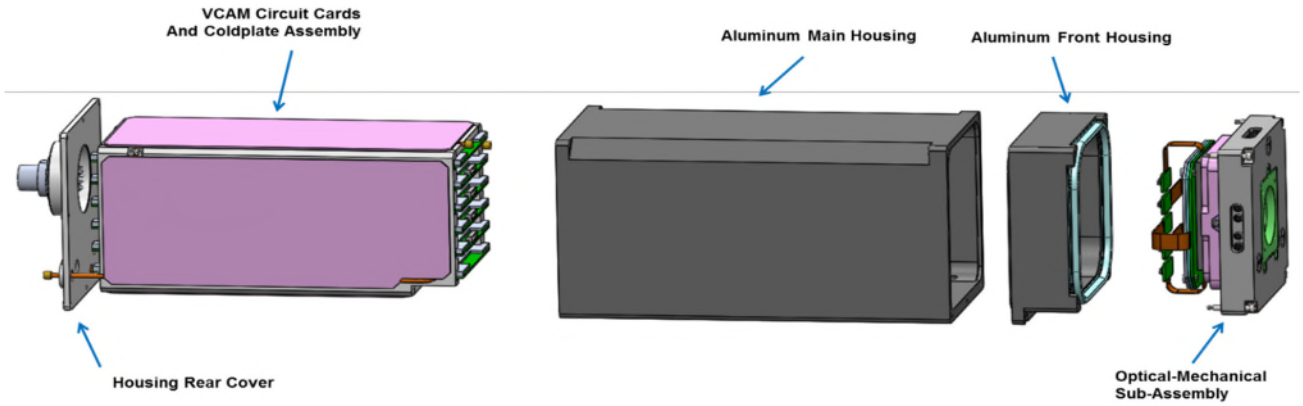

Figure 11: Preliminary opto-mechanical design of VCAM

The cold plate assembly will carry away the heat generated by VCAM using a coolant such as a refrigerant that is maintained at the -30 °C interior temperature of the NFIRAOS optical enclosure. While most of the coolant flow will be evaporated to cool the camera, a small amount will remain in liquid form to ensure the return coolant lines are isothermal with respect to the NFIRAOS interior. Because of the low operating temperature, all the VCAM electronics are designed for operation to -40 °C by use of industrial temperature range components.

The CCD and the lenslet array are mounted in an opto-mechanical sub-assembly that is attached to the main housing by a front housing section that separates from the main housing to allow access to the connections between the electronics circuit boards and the circuit board for the CCD. This circuit board provides a zero insertion force socket for the 480 pin PGA package of the CCD. The opto-mechanical assembly is made of Invar-36 to provide a match to the thermal expansion properties of the Kovar CCD package. The lenslet array is made of fused silica and the array is mounted so that stress in the lenslet array due to the thermal mismatch with the Invar-36 is properly managed. The front housing also provides a flexible seal to allow limited independent motion of the opto-mechanical assembly for optical alignment with NFIRAOS. The performance of the Shack Hartmann wavefront sensor depends on proper alignment of the lenslet array to the CCD, and the optomechanical assembly provides the adjustments needed to allow precision alignment of the lenslet array to the CCD.

To minimize the impact of the need to remove and replace a camera in NFIRAOS, VCAM is provided with datum features on the opto-mechanical assembly that mate repeatably with features on the NFIRAOS side of the interface. The VCAM CCD, and in turn the lenslet array, are precisely aligned to these datum features during assembly and test. With sufficiently precise alignment in each VCAM all the cameras will be interchangeable without requiring any optical realignment in NFIRAOS.

The LGS version of VCAM uses six circuit boards, a control and timing board, a clock and bias board, and four 32 channel video boards. The boards stack on top of each other with interconnections made through high density stacking connectors. Almost all of the components are surface mount devices. Each board is designed to sit in the camera's cold plate assembly with a cooling plate on top of it that is coupled to the components with thermal foam. The cooling plates are machined as needed to provide recesses to accommodate the taller components. Wedge locking devices hold each card and the cooling plates in the cold plate assembly and ensure good thermal contact between the cooling plates and the cold plate assembly.

Figure 12 shows a component side view of the prototype VCAM control and timing board. At the left side of the figure connections are provided for testing and for the power to the TEC in the CCD package. To the right are low noise power supply circuits for the digital logic and for the analog circuitry on the timing and video boards. VCAM is supplied with DC power from a remotely mounted AC to DC power supply located outside of the NFIRAOS optical enclosure. The DC power supply voltages are then locally regulated using very low noise switching supplies to provide the various voltages required for the logic and analog circuitry. Continuing to the right the large device is an FPGA that provides the logic needed to multiplex the video board outputs onto the 10 Gbit/s data link to the RTC. This FPGA also orchestrates the timing of the readout process and implements the media access controller (MAC) for the 10 Gbit/s data link.

Below the FPGA is the control processor. This is a 32 bit flash memory microcontroller running a real time operating system. The microcontroller includes the MAC for the 100 Mbit/s link used by the NFIRAOS component controller to control the operation of VCAM. At the far right of the board there are two small form factor pluggable (SFP) cages for the fiber optic transceivers employed for optical communications by the two data links. Just below the upper SFP cage is a SMA connector that supports a frame trigger signal for timing of camera exposures. Between the two SFP cages on the back of the board is the stacking connector to the clock and bias board, and a connector for the DC power input from the external power connector on the rear panel of the camera. The control and timing board provides for complete reprogramming of the microcontroller program via a boot strap loader as well as reprogramming of the CCD readout timing and the clock and bias voltages. The microcontroller monitors all of the power supply voltages, the supply and return coolant temperatures and the temperature inside of VCAM. The microcontroller also implements a servo loop that controls the temperature of the CCD via the TEC.

Figure 12: Prototype VCAM control and timing board

Figure 13 shows a component side view of the prototype VCAM clock and bias board. This board provides adjustable levels for the 66 clocks required by the CCID87, along with various bias voltages required for device operation. All of the voltages are adjustable by the VCAM controller using digital to analog converters on the clock and bias board. The connections to the CCD circuit board are made through a flex circuit cable connected to the left side of the board. At the right hand end of the board the stacking connector to the control and timing board can be seen with the connector to the first video board located underneath this connector on the bottom of the board.

Figure 14 shows a component side view of the prototype VCAM 32 channel video board. This board provides 32 channels of correlated double sampling followed by 18 bit high speed analog to digital converters (ADCs). Four levels of gain adjustment are provided by selection of 16 bits out of the 18. The output of the 32 ADCs are transmitted by a serial data channel running at 3.125 Gbits/s. Multiplexing of the ADCs is handled by an FPGA located at the right side of the board.

The 32 video inputs are connected to the CCD circuit board through a flex circuit cable connected to the left side of the board. At the right hand end of the board, the stacking connector to the clock and bias board can be seen with the connector to the next video board located underneath this connector on the bottom of the board. The remaining three video boards required for the CCID87 are stacked beneath the first video board.

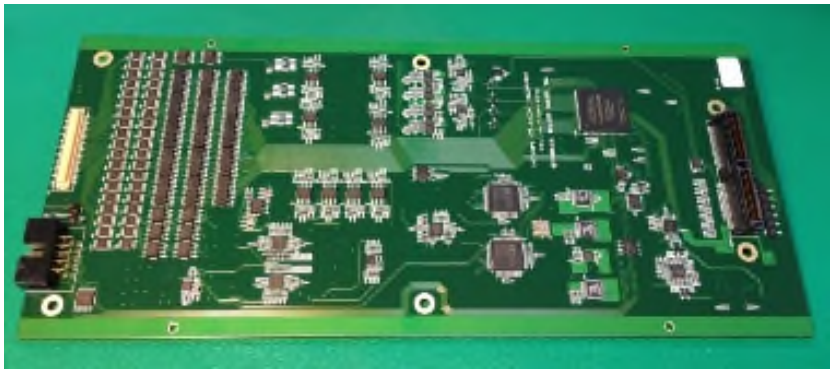

Figure 13: Prototype VCAM clock and bias board

Figure 14: Prototype VCAM 32 channel video board

As noted earlier VCAM is designed for use with the CCID87 detector for the NFIRAOS LGS wavefront sensors, and for use with the CCID74 detector for the NFIRAOS NGS wavefront sensor. The CCID74 has 64 video outputs, so the NGS VCAM configuration will only require two video boards but is otherwise electrically identical to the LGS version. The CCID74 will be packaged in the same package as that used for the CCID87. The NGS wavefront sensor uses a pyramid configuration for wavefront sampling, so the NGS VCAM will not have a lenslet array but is otherwise mechanically identical to the LGS version of VCAM.

VCAM Specifications

The specifications of VCAM are summarized in Table 2.

• 128 video inputs, 16 bit CDS	• Safe power-on/off sequencing of CCD voltages
• ≤ 1 e- camera noise at a 3.6 MHz pixel clock rate	• Monitoring of all supply voltages, internal temperature and coolant supply and return
• 5 MHz maximum pixel clock rate	• Closed loop TEC controller for the detector
• 66 clock outputs and 10 bias outputs	• Total power consumption < 100 W
• 10 Gbit/s Ethernet (10GBASE-SR) data interface	• Refrigeration cooled, operating ambient temperature range -30.5 to +25 °C
• 100 Mbit/s Ethernet (100Base-FX) for control	• 140 mm x 135 mm x 361 mm (H x W x D, not including external connections)
• Fully reprogrammable via the control interface	• Mass ≤ 20 kg

Table 2: VCAM summary specifications

4. CONCLUSIONS

VCAM has successfully completed its preliminary design review and a 32 channel prototype of the electronics is currently being tested with the CCID74 detector. An image from early in the testing process is shown in Figure 15. This image is from an engineering grade CCID74 operating at room temperature. The channel offsets and bias voltages have not yet been optimized.

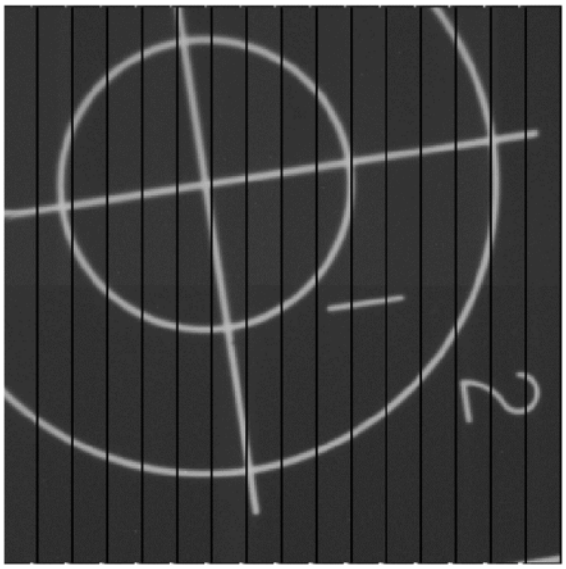

Figure 15: Early test image from VCAM using an engineering grade CCID74 (the vertical black lines are deliberate to allow easier identification of individual video channels)

The final design of VCAM is expected to start later in calendar 2017 followed by construction of a pre-production prototype. After acceptance the production of 8 VCAM units will commence. Six of these will be used for the LGS wavefront sensors, one for the NGS wavefront sensor, and one as a spare to support both camera configurations.

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